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Title:

METHOD OF FORMING COPPER WIRING IN SEMICONDUCTOR DEVICE

Sang Kyun Park

Samsungraemian Apt. 111-803,
Samgeoma-eul, 629,
Mabuk-Ri, Kusung-Myun, Yongin-Shi,
Kyungki-Do,
Republic of Korea

METHOD OF FORMING COPPER WIRING IN SEMICONDUCTOR DEVICE

BACKGROUND

1. Field of the Invention

[0001] The present invention relates to a method of forming a copper wiring in a semiconductor device and, more particularly, to a method of forming a copper wiring in a semiconductor device capable of preventing an electrical short condition between neighboring copper wirings and facilitating subsequent processes through surface polishing, by prohibiting electro-migration and stress migration of copper in the copper wiring formed within a damascene pattern.

2. Discussion of Related Art

[0002] Generally, as the semiconductor industry shifts to an ultra large-scale integration (ULSI) level, the geometry of the device continues to be narrowed to a sub-half-micron region. In view of improved performance and reliability, the circuit density is gradually increased. Copper has a high resistance to electro-migration (EM) since it has a higher melting point than aluminum. Thus, copper can improve reliability of the device. Further, copper can increase a signal transfer speed since it has a low resistivity. For this reason, in forming a metal wiring in a semiconductor device, copper has been used as an interconnection material useful for an integration circuit.

[0003] A method of burying copper that may be used currently includes a physical vapor deposition (PVD) method/a reflow method, a chemical vapor deposition (CVD) method, an electroplating method, an electroless-plating method, and the like. Preferred methods of them are the electroplating method and the CVD method, both of which have a relatively good copper burial characteristic.

[0004] While copper is used as a material of a metal wiring, a damascene scheme for simultaneously forming a via contact hole for electrical connection to a lower layer and a trench in which the metal wiring is located, has been widely used along with a process of forming a copper wiring in a semiconductor device. A low-dielectric insulating material having a low dielectric constant is used as an interlayer insulating film in which a damascene pattern will be formed.

[0005] In order to form a copper wiring in the damascene pattern having the via contact hole and the trench, copper is buried into the damascene pattern through several methods and the buried copper layer is then polished by a chemical mechanical polishing (CMP) process, so that the buried copper layer is isolated from neighboring copper wirings.

[0006] Fig 1 is a sectional view for explaining the method of forming the copper wiring in the semiconductor device according to a prior art.

[0007] A first interlayer insulating film 12 and an anti-polishing layer 13 are formed on a substrate 11. The anti-polishing layer 13 and the first interlayer insulating film 12 are etched by a damascene scheme to form a damascene pattern 14.

[0008] A copper anti-diffusion conductive film 15 is formed along the surface of the anti-polishing layer 13 including the damascene pattern 14. A copper layer is formed enough to sufficiently bury the damascene pattern 14. A CMP process is then performed until the anti-polishing layer 13 is exposed, thus forming a copper wiring 16 within the damascene pattern 14. Thereafter, a copper anti-diffusion insulating film 100 and a second interlayer insulating film 17 are formed on the entire structure including the copper wiring 16.

[0009] In the above-mentioned method, in order to prevent diffusion of copper elements from the copper wiring 16 to the outside, the copper wiring 16 is sealed using the copper anti-diffusion conductive film 15 and the copper anti-diffusion insulating film 100. In the device having the copper wiring 16 formed by a conventional method, however, most of defective wirings generated due to electro-migration and stress migration takes place at the interface between the copper anti-diffusion insulating film 100 and the copper anti-diffusion conductive film 15, as indicated by an arrow "A". This condition is caused by a lack in the bondability between the copper anti-diffusion insulating film 100 and the underlying layers 13, 15 and 16.

SUMMARY OF THE INVENTION

[0010] The present invention is directed to provide a method of forming a copper wiring in a semiconductor device capable of enhancing electrical properties of the device, preventing an electrical short condition between neighboring copper wirings and facilitating subsequent processes through

surface polishing, by prohibiting electro-migration and stress migration of copper in the copper wiring formed within a damascene pattern.

[0011] According to a preferred embodiment of the present invention, there is provided a method of forming a copper wiring in a semiconductor device, including the steps of providing a substrate in which a damascene pattern is formed in an interlayer insulating film, forming a copper anti-diffusion conductive film and a copper layer on the entire structure including the damascene pattern, forming a copper wiring by means of a chemical mechanical polishing process, wherein the surface of the copper wiring is lower than the surface of the interlayer insulating film, and forming a copper anti-diffusion insulating film on the entire structure including the top of the copper wiring.

[0012] In the above, the copper anti-diffusion insulating film is formed by covering materials such as methyl, benzochlorobutane, polyimide, arylether and hydrogen silsesquioxane, which contain Si, C and N in a type of a sol or gel, and then performing an annealing process in order to densify the covered film. In the above, the annealing process is performed using an inert gas such as N_2, Ar, H_2 or He or a mixed gas of them at a temperature of 100 to 500℃.

[0013] According to another embodiment of the present invention, there is provided a method a method of forming a copper wiring in a semiconductor device, including a first step of providing a substrate in which a damascene pattern is formed in an interlayer insulating film, a second step of forming a copper anti-diffusion conductive film and a copper layer on the entire structure including the damascene pattern, a third step of forming a copper wiring by

means of a chemical mechanical polishing process, wherein the surface of the copper wiring is lower than the surface of the interlayer insulating film, and a fourth step of plasma-processing the surface of the copper wiring and then forming a selective copper anti-diffusion conductive film on the plasma-processed surface.

[0014] In the above, the third step includes the steps of overly performing a chemical mechanical polishing process so that the top surface of the copper wiring is concaved and formed lower than the surface of the interlayer insulating film, and performing an annealing process so that the top surface of the copper wiring is changed from the concave shape to a convex shape while stabilizing the copper wiring.

[0015] The annealing process may be performed using an inert gas such as N_2, Ar, H_2 or He or a mixed gas of them at a temperature of 100 to 500℃, or may be performed using an inert gas of N_2, Ar, H_2 or He or a mixed gas of them or in a vacuum state at a temperature range of 200 to 700℃ for 1 to 5 minutes in a rapid thermal annealing process.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] Fig 1 is a sectional view for explaining a method of forming a copper wiring in a semiconductor device according to a prior art;

[0017] Figs. 2A to 2C are sectional views for explaining a method of forming a copper wiring in a semiconductor device according to an embodiment of the present invention; and

[0018] Figs. 3A to 3C are sectional views for explaining a method of forming a copper wiring in a semiconductor device according to another embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0019] Now the preferred embodiments according to the present invention will be described with reference to the accompanying drawings. Since preferred embodiments are provided for the purpose that the ordinary skilled in the art are able to understand the present invention, they may be modified in various manners and the scope of the present invention is not limited by the preferred embodiments described later.

[0020] Figs. 2A to 2C are sectional views for explaining a method of forming a copper wiring in a semiconductor device according to an embodiment of the present invention.

[0021] Referring to Fig. 2A, a first interlayer insulating film 22 and an anti-polishing layer 23 are formed on a substrate 21. The anti-polishing layer 23 and the first interlayer insulating film 22 are etched by a damascene scheme to form a damascene pattern 24. A copper anti-diffusion conductive film 25 is then formed along the surface of the anti-polishing layer 23 including the damascene pattern 24. A copper layer is formed enough to sufficiently bury the damascene pattern 24. The copper layer is formed by plating copper directly on the copper anti-diffusion conductive film 25, or forming a copper seed layer (not shown) on the copper anti-diffusion conductive film 25 and then plating copper. The copper seed layer is formed

by means of an ionized PVD, CVD, or electroless copper plating method with a thickness in the range of 50~300nm. Thereafter, a CMP process is performed to form a copper wiring 26 within the damascene pattern 24. In this case, the CMP process is overly performed so that the top surface of the copper wiring 26 is concaved and is lower than the surface of the first interlayer insulating film 22 neighboring it. After the CMP process is completed, a cleaning process is performed.

[0022] In the above, the first interlayer insulating film 22 is formed using a material having a low dielectric constant in order to solve problems due to parasitic capacitance between the wirings. For example, the first interlayer insulating film 22 may be formed using a material in which H, F, C, CH_3, etc. are partially mixed in SiO_2 series having a dielectric constant of 1.5 to 4.5, an organic material such as SiLK™ product, Flare™ product, etc., which have C-H as a basic structure, and a porous material whose porosity is increased in order to lower the dielectric constant of the above materials.

[0023] The anti-polishing layer 23 may be formed using oxides not containing carbon. Further, the anti-polishing layer 23 may be formed using silicon nitride and silicon nitride oxide containing nitrogen or a series of silicon carbide containing carbon, by means of a chemical vapor deposition (CVD) method so that they have a copper anti-diffusion property.

[0024] The copper anti-diffusion conductive film 25 may be formed by one of ionized PVD TiN, CVD TiN, MOCVD TiN, ionized PVD Ta, ionized PVD TaN, CVD Ta, CVD TaN and CVD WN, or a combination of them.

[0025] The cleaning process may be performed using a cleaning agent containing a small amount of nitric acid, etc. so that the surface of the copper wiring 26 is further lower than the surface of the first interlayer insulating film 22 neighboring it.

[0026] By reference to Fig. 2B, a first annealing process is performed to stabilize the copper wiring 26. In the case, the top surface of the copper wiring 26 is changed from the concave shape to a convex shape so as to minimize surface energy due to heat.

[0027] In the above, the first annealing process is performed in two methods. The first method is performed using an inert gas of N_2, Ar, H_2, or He, etc., or a mixed gas of them at a temperature range of 100 to 500℃. The second method is performed using an inert gas of N_2, Ar, H_2, or He, etc., or a mixed gas of them or in a vacuum state at a temperature range of 200 to 700℃ for 5 or lower minutes, preferably for 1 to 5 minutes in a rapid thermal annealing process.

[0028] With reference to Fig. 2C, in order to remove impurities such as an oxide layer generated on the surface of the copper wiring 26, a plasma process is performed and a copper anti-diffusion insulating film 200 is formed on the entire structure including the top surface of the copper wiring 26 having the convex shape. A second interlayer insulating film 27 is then formed on the entire structure including the copper anti-diffusion insulating film 200.

[0029] In the above, the plasma processing is carried out using a mixed gas containing nitrogen and hydrogen, a gas of a series of ammonia, or a

mixed gas of hydrogen/an inert gas not containing nitrogen as an atmosphere gas at a temperature range of 100 to 350℃.

[0030] In the above, the copper anti-diffusion insulating film 200 is formed using a material for which surface polishing can be easily performed, while having a copper anti-diffusion property. That is, the copper anti-diffusion insulating film 200 is formed by covering source materials such as methyl, benzochlorobutane, polyimide, arylether, hydrogen silsesquioxane, and the like, which contain Si, C, N, etc. in a type of a sol or gel having a good fluidity property, in a thickness of 300Å or more, preferably in the range of 300 to 700Å by means of a spin-on deposition mode, and then performing a second annealing process to densify the covered film. In this case, the second annealing process is performed in two methods. The first method is performed using an inert gas of N_2, Ar, H_2, He, etc., or a mixed gas of them at a temperature range of 100 to 500℃, for 1 or more minute, preferably 1 to 5 minutes. The second method is performed in a vacuum state at a temperature range of 100 to 500℃ for 1 or over minutes, preferably for 1 to 5 minutes.

[0031] In case of a multi-layer metal wiring structure, it is preferred that the second interlayer insulating film 27 is formed using a material having a low dielectric constant in order to solve the problems due to the parasitic capacitor among the wirings as in the mentioned first interlayer insulating film 22. In case of a single layer metal wiring structure, however, it may be preferred that the second interlayer insulating film 27 is formed using a material that is usually used to form an interlayer insulating film of a semiconductor device.

[0032] Figs. 3A to 3C are sectional views for explaining a method of forming a copper wiring in a semiconductor device according to another embodiment of the present invention.

[0033] Referring to Fig. 3A, a first interlayer insulating film 32 and an anti-polishing layer 33 are formed on a substrate 31. The anti-polishing layer 33 and the first interlayer insulating film 32 are etched by a damascene scheme to form a damascene pattern 34. A copper anti-diffusion conductive film 35 is then formed along the surface of the anti-polishing layer 33 including the damascene pattern 34. A copper layer is formed enough to sufficiently bury the damascene pattern 34. Thereafter, a CMP process is performed to form a copper wiring 36 within the damascene pattern 34. In this case, the CMP process is overly performed so that the top surface of the copper wiring 36 is concaved and is lower than the first interlayer insulating film 32 neighboring it. After the CMP process is completed, a cleaning process is performed.

[0034] In the above, the first interlayer insulating film 32 is formed using a material having a low dielectric constant in order to solve problems due to parasitic capacitance between the wirings. For example, the first interlayer insulating film 32 may be formed using a material in which H, F, C, CH_3, etc. are partially mixed in SiO_2 series having a dielectric constant of 1.5 to 4.5, an organic material such as SiLK™ product, Flare™ product, etc., which have C-H as a basic structure, and a porous material whose porosity is increased in order to lower the dielectric constant of the above materials.

[0035] The anti-polishing layer 33 may be formed using oxides not containing carbon. Further, the anti-polishing layer 33 may be formed using silicon nitride and silicon nitride oxide containing nitrogen or a series of silicon carbide containing carbon, by means of a CVD method so that they have a copper anti-diffusion property.

[0036] The copper anti-diffusion conductive film 35 may be formed by one of ionized PVD TiN, CVD TiN, MOCVD TiN, ionized PVD Ta, ionized PVD TaN, CVD Ta, CVD TaN and CVD WN, or a combination of them.

[0037] The cleaning process may be performed using a cleaning agent containing a small amount of nitric acid, etc. so that the surface of the copper wiring 36 is further lower than the surface of the first interlayer insulating film 32 neighboring it.

[0038] By reference to Fig. 3B, an annealing process is performed to stabilize the copper wiring 36. In the case, the top surface of the copper wiring 36 is changed from the concave shape to a convex shape so as to minimize surface energy due to heat.

[0039] In the above, the annealing process is performed in two methods. The first method is performed using an inert gas of N_2, Ar, H_2, He, etc. or a mixed gas of them at a temperature range of 100 to 500℃. The second method is performed using an inert gas of N_2, Ar, H_2, He, etc. or a mixed gas of them or in a vacuum state at a temperature range of 200 to 700℃ for 5 or lower minutes, preferably for 1 to 5 minutes in a rapid thermal annealing process.

[0040] With reference to Fig. 3C, in order to remove impurities such as an oxide layer generated on the surface of the copper wiring 36, plasma is

processed and a selective copper anti-diffusion insulating film 300 is formed on the entire structure including the top surface of the copper wiring 36 having the convex shape. A second interlayer insulating film 37 is then formed on the entire structure including the copper anti-diffusion insulating film 300.

[0041] In the above, the plasma processing is carried out using a mixed gas containing nitrogen and hydrogen, a gas of a series of ammonia, or a mixed gas of hydrogen/an inert gas not containing nitrogen as an atmosphere gas at a temperature range of 100 to 350℃.

[0042] It is required that the selective copper anti-diffusion conductive film 300 be formed within the damascene pattern 34 without causing a step with the first interlayer insulating film 32 neighboring it. Furthermore, the selective copper anti-diffusion conductive film 300 is formed in two methods. The first method is performed using a metal having a high melting point such as W, Ti, Ta, etc or a compound such as Ni, Co, P, B, etc. by means of a selective electroless plating method. The second method is performed by means of a selective CVD method.

[0043] In case of a multi-layer metal wiring structure, it is preferred that the second interlayer insulating film 37 is formed using a material having a low dielectric constant in order to solve the problems due to the parasitic capacitor among the wirings as in the mentioned first interlayer insulating film 32. In case of a single layer metal wiring structure, however, it may be preferred that the second interlayer insulating film 37 is formed using a material that is usually used to form an interlayer insulating film of a semiconductor device.

[0044] According to one embodiment of the present invention described above, a copper anti-diffusion insulating film is formed not only within a damascene pattern but also on the entire structure, thus serving as a barrier to prohibit electro-migration and stress migration of copper. It is thus possible to improve reliability of a wiring. Furthermore, the whole plane including an upper side of a copper wiring is polished without a step to facilitate a photolithography process, an etch process, etc. that are subsequent performed. It is therefore possible to improve reliability in process.

[0045] According to another embodiment of the present invention described above, the top surface of a copper wiring is lower than the surface of an interlayer insulating film of a low dielectric constant neighboring it and a selective copper anti-diffusion conductive film on the copper wiring is formed within a damascene pattern without causing a step with an interlayer insulating film of a dielectric constant neighboring it. As the selective copper anti-diffusion conductive film serves as a barrier to prohibit electro-migration and stress migration of copper, it is possible to improve reliability of the wiring. Furthermore, the selective copper anti-diffusion conductive film is formed only within the damascene pattern to prevent an electrical short condition among neighboring copper wirings. It is thus possible to improve wiring fail. Therefore, the present invention has advantages that it can enhance electrical properties and reliability of devices and makes it possible to realize higher-integration of the device.

[0046] Although the foregoing description has been made with reference to the preferred embodiments, it is to be understood that changes and

modifications of the present invention may be made by the ordinary skilled in the art without departing from the spirit and scope of the present invention and appended claims.